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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,247	11/08/2001	Min Kim	SEC.853	5037

7590 09/25/2002
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EXAMINER

GUERRERO, MARIA F

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 09/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/986,247

Applicant(s)

KIM ET AL.

Examiner

Maria Guerrero

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 July 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 1-10 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. This Office Action is in response to the Preliminary amendment filed November 8, 2001 and the Election filed July 2, 2002.

Claims 1-21 are pending.

Election/Restrictions

2. Claims 1-10 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.

Applicant's election without traverse of Group II claims 11-21 in Paper No. 5 is acknowledged.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5. Claim 11 is objected to because of the following informalities: claim 11 recites "a method of manufacturing trench isolation structure of a semiconductor device". It is suggested to insert "a" before the term trench and to replace the term "of" by "on", after the term "structure". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 recites the limitation "between the liner" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 11, 13, 15-16, 17, 19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zdebel et al. (U.S. 5,004,703) in view of Hashimoto et al. (U.S. 6,027,983).

Zdebel et al. teaches sequentially forming a pad oxide layer and a hard mask layer on a semiconductor substrate, patterning the hard mask layer and the pad oxide layer by photolithography to form a hard mask pattern and a pad oxide pattern, etching a portion of the substrate using the hard mask pattern as mask to thereby form a shallow trench (Fig. 1, col. 2, lines 30-50). Zdebel et al. teaches forming a thermal oxide layer along inner walls of the semiconductor substrate that define the shallow

trench, etching away portions of the thermal oxide layer and the semiconductor substrate using the hard mask pattern as mask to extend the shallow trench deeper into the semiconductor substrate (Fig. 4-5, col. 2, lines 49-51, col. 3, lines 30-35).

In addition, Zdebel et al. teaches forming a thermal oxide layer on a portion of the upper surface of the semiconductor substrate where a trench isolation layer will be formed; etching away portions of the thermal oxide layer and the semiconductor substrate using the hard mask pattern as a mask to form the trench (Fig. 3-5, col. 3, lines 22-35).

Furthermore, Zdebel et al. shows forming a buffer layer over the trench, filling the trench with a first oxide layer. Zdebel et al. teaches forming a liner between the buffer layer and the first oxide layer (col. 3, lines 40-45, col. 4, lines 65-68). Zdebel et al. discloses the semiconductor substrate having a silicon-on-insulator (SOI) structure comprising a silicon substrate, a buried oxide layer and a silicon layer disposed atop the other, and etching the semiconductor substrate at a location within the silicon layer in forming the shallow trench (Fig. 1, col. 2, lines 15-50).

Zdebel et al. does not specifically show the trench being a deep trench, planarizing the resulting structure, and removing the hard mask pattern. However, Zdebel shows that trench depth is application specific and suggested forming a planar isolation structure (col. 3, lines 30-35, 47-50). In addition, Hashimoto et al. shows the step of planarizing after filling the deep trench and removing the hard mask as conventional in the art (Fig. 13, col. 2, lines 45-57, col. 11, lines 1-3).